Notice of Allowability	Application No.	Applicant(s)	
	10/631,824	MONTAGNE ET AL.	
	Examiner	Art Unit	
	MATTHEW C. TABLER	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *interview on 10 November 2009*.

2. ☒ The allowed claim(s) is/are *43-58*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *11/10/09* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/M. C. T./
Examiner, Art Unit 2819

DETAILED ACTION

This office action is in response to interview held on November 10, 2009. Currently, claims 1, 2-7, 9-10, 12-15, 35-36, and 40-42 have been canceled by examiner's amendment and new claims 43-58 have been allowed.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Ross Dannenberg on November 10th, 2009.

The application has been amended as follows:

Claims 1-42 are canceled.

Claim 43 (New) An integrated circuit, comprising:

a reconfigurable interconnect portion;

a data processing portion coupled to the reconfigurable interconnect portion, the data processing portion configured to provide a bit pattern to the reconfigurable interconnect portion to load a configuration of the reconfigurable interconnect portion; and

a storage unit coupled to the data processing portion, the storage unit including a configuration bit look-up table,

wherein the data processing portion is configured to extract a set of bits from the configuration bit look-up table to map a common plurality of inputs of the reconfigurable interconnect portion to a plurality of outputs of the reconfigurable interconnect portion.

Claim 44 (New) The integrated circuit of claim 43, wherein the integrated circuit includes a second reconfigurable interconnect portion, and the configuration bit look-up table is configured to allow the data processing portion to extract a first set of configuration bits representing the bit pattern and to extract a second set of configuration bits representing a second bit pattern to load a second configuration of the second reconfigurable interconnect portion, wherein the second set is a subset of the first set.

Claim 45 (New) The integrated circuit of claim 43, wherein the reconfigurable interconnect portion comprises a switching matrix.

Claim 46 (New) The integrated circuit of claim 43, wherein reconfigurable interconnect portion comprises a multiplexer.

Claim 47 (New) The integrated circuit of claim 45, wherein the switching matrix includes a control signal input configured to select between two inputs to connect to an output.

Claim 48 (New) The integrated circuit of claim 43, wherein the reconfigurable interconnect portion comprises a pair of transistors.

Claim 49 (New) The integrated circuit of claim 43, wherein the reconfigurable interconnect portion comprises a plurality of memory elements, each memory element connected to at least one switch of the reconfigurable interconnect portion.

Claim 50 (New) The integrated circuit of claim 43, wherein the bit pattern is derived from the configuration bit look-up table.

Claim 51 (New) The integrated circuit of claim 43, wherein the configuration bit look-up table comprises a plurality of rows of configuration bits.

Claim 52 (New) The integrated circuit of claim 51, wherein the storage unit is coupled to the data processing portion by a plurality of address lines for accessing the rows of configuration bits stored within the storage unit.

Claim 53 (New) The integrated circuit of claim 52, wherein the storage unit further comprises programming instructions configured for accessing the configuration bit look-up table, wherein the programming instructions are further configured for extracting a subset of configuration bits from the configuration bit look-up table.

Claim 54 (New) The integrated circuit of claim 43, wherein the data processing portion is configured to map a first input of the common plurality of inputs of the reconfigurable interconnect portion to a first output of the plurality of outputs of the reconfigurable interconnect portion in response to a first command.

Claim 55 (New) The integrated circuit of claim 54, wherein the data processing portion is configured to map a second input of the common plurality of inputs of the reconfigurable interconnect portion to a second output of the plurality of outputs of the reconfigurable interconnect portion in response to the first command.

Claim 56 (New) The integrated circuit of claim 54, wherein the data processing portion is configured to map a second input of the common plurality of inputs of the reconfigurable interconnect portion to a second output of the plurality of outputs of the reconfigurable interconnect portion in response to a second command.

Claim 57 (New) The integrated circuit of claim 54, further comprising a second reconfigurable interconnect portion, and wherein the data processing portion is configured to map a first input of the second reconfigurable interconnect portion to a first output of the second reconfigurable interconnect portion in response to a second command.

Claim 58 (New) An integrated circuit, comprising:

a reconfigurable interconnect portion;

a data processing portion coupled to the reconfigurable interconnect portion, the data processing portion configured to provide a bit pattern to the reconfigurable interconnect portion to load a configuration of the reconfigurable interconnect portion; and

a storage unit coupled to the data processing portion, the storage unit including a look-up table,

wherein the look-up table is confgured to allow the data processing portion to extract a first set of bits representing the bit pattern and to extract a second set of bits representing a second bit pattern to load a second configuration of a second reconfigurable interconnect portion,

wherein the second set is a subset of the first set,

wherein the extraction of the second set of bits from the look-up table maps a common plurality of inputs of the reconfigurable interconnect portion to a plurality of outputs of the reconfigurable interconnect portion.

Allowable Subject Matter

Claims 43-58 are allowed.

The following is an examiner's statement of reasons for allowance: After a thorough search of related prior, the circuit in independent claims 43 and 58 could not be found. More specifically, the structure of claim 43 in combination with 'a data processing portion coupled to the reconfigurable interconnect portion, the data processing portion configured to provide a bit pattern to the reconfigurable interconnect portion to load a configuration of the reconfigurable interconnect portion, and wherein the data processing portion is configured to extract a set of bits from the configuration bit look-up table to map a common plurality of inputs of the reconfigurable interconnect portion to a plurality of outputs of the reconfigurable interconnect portion' could not be found within a reference(s) or the combination thereof.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MATTHEW C. TABLER whose telephone number is (571)270-1567. The examiner can normally be reached on Monday through Friday 8:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rexford Barnie can be reached on (571) 277-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Vibol Tan/
Primary Examiner, Art Unit 2819

/M. C. T./
Examiner, Art Unit 2819
November 10, 2009